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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,903	10/19/2001	Markus Schetelig	1117.40737X00	7306
20457	7590	05/12/2005		EXAMINER
				KIM, KEVIN
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/981,903	SCHETELIG ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Kevin Y. Kim	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 19 October 2001.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,5,8,9,11,12 is/are rejected.  
 7) Claim(s) 3,4,6,7,10,13-16 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 19 October 2001 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/19/01, 1/14/03, 6/24/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1.

***Specification***

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use. In this applications, the suggested headings are missing.

**Arrangement of the Specification**

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or  
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
- (f) BACKGROUND OF THE INVENTION.
  - (1) Field of the Invention.
  - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

***Drawings***

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2. The drawings are objected to because Figs. 1, 2 and 4 fails to label the rectangles in the block diagram as to their respective functions for readily identification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1,2,5,8,9,11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al (US 5,729,571) in view of Carsello et al (6,529,566)

Claim 1.

Park et al discloses a method for identifying a data packet in a data stream (see Fig.1) comprising the steps of;

comparing “k-bit word” in the input signal to “an expected k-bit synchronization word” (Unique word) to determine a correlation value (see correlators 115,123, etc), and generating a packet identification signal if the correlation value is greater than a predetermined threshold value (see comparator 135).

But Park et al fails to teach calculating “the d.c. voltage quota” for a demodulated signal and determining the bit values of the k-bit word as a function of the d.c. voltage quota.

Carsello et al teaches calculating the average value of input bits, i.e., “the d.c. voltage quota,” and determining the bit values of input bit stream using the average value for facilitating the bit decision. See Fig.3 and col. 4,lines 18-27 and col.1, lines 35-41. Thus, it would have been obvious to one skilled in the art at the time the invention was made to calculate “the d.c.

voltage quota” for a demodulated signal output from the baseband demodulator of Iwasaki and determining the bit values of the k-bit word as a function of the d.c. voltage quota, as taught by Carsello et al for the purpose of providing more accurate bit value even when the received signal has been subject to smearing and noise.

Claims 2 and 5.

Iwasaki discloses scanning the input signal to generate a sequence of values (see A/D 114), a selected number of which would be provided as input to the “d.c. voltage quota” generator as taught by Carsello et al.

Claim 8.

Carsello teaches using two bits of input samples and calculating the average as the d.c. voltage. And since the synch code is random, the number two would correspond to “areas in the expected k bit synchronization word with substantially have the same number of bits with the value “0” and bits with the value “1”.

Claim 9.

Carsello teaches using two sequential bits of input samples for calculating the d.c. voltage. However, it is obvious using a group of bits “in direct succession to one another, which correspond to several successive symbols” since more samples would yield a more accurate average signal level, i.e., the d.c. voltage quota.

Claim 11.

Park et al discloses a device for identifying a data packet in a data stream (see Fig.1) comprising;

“a comparison and correlation calculating circuit” comparing “k-bit word” in the input signal to “an expected k-bit synchronization word” (PN code) to determine a correlation value (see correlators 115,123, etc), and

“a correlation value comparison circuit” for generating a packet identification signal if the correlation value is greater than a predetermined threshold value (see comparator 135).

But Park et al fails to teach “a delay line,” “a d.c. voltage quota determining circuit” and “a decoding circuit” for allocating bit values to scanned values.

Carsello et al teaches “a delay line which has a number of storage places” (302), “a d.c. voltage quota determining circuit” (306,310) for calculating the average value of input bits, i.e., “the d.c. voltage quota,” and “a decoding circuit” (312) for allocating bit values to scanned values for facilitating the bit decision. See Fig.3 and col. 4,lines 18-27 and col.1, lines 35-41. Thus, it would have been obvious to one skilled in the art at the time the invention was made to add “a delay line,” “a d.c. voltage quota determining circuit” and “a decoding circuit” to the input of correlators of Park et al for the purpose of providing more accurate bit value even when the received signal has been subject to smearing and noise, as taught by Carsello et al.

Claim 12.

Though Carsello describes one storage place it would have been obvious to provide a plurality of storage places to provide more accurate average level of the received signals.

*Allowable Subject Matter*

6. Claims 3,4,6,7,10,13,14,15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sano et al (US 6,246,735) teaches "d.c. voltage quota" computing device. See Fig.9.  
Iwasaki (US 5,463,401) teaches a synch code detector. See Fig.1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Y. Kim whose telephone number is 571-272-3039. The examiner can normally be reached on 8AM --5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KEVIN KIM  
PATENT EXAMINER  
